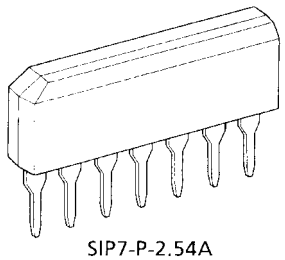
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8030S,TA8030F

WATCHDOG TIMER

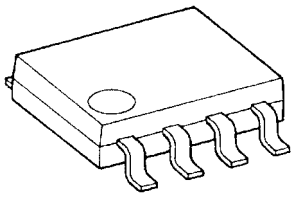
The TA8030S TA8030F is a system reset IC for 5V supply voltage system. It is specially designed for microcomputer systems. It incorporates a watchdog timer for monitoring microcomputer operation and has many reset functions, including a reset timer output which will be given at power-on and another reset output which will be given when the supply voltage drops. With these functions, it helps build up a reliable system.

TA8030S



SIP7-P-2.54A

TA8030F



SOP8-P-225-1.27

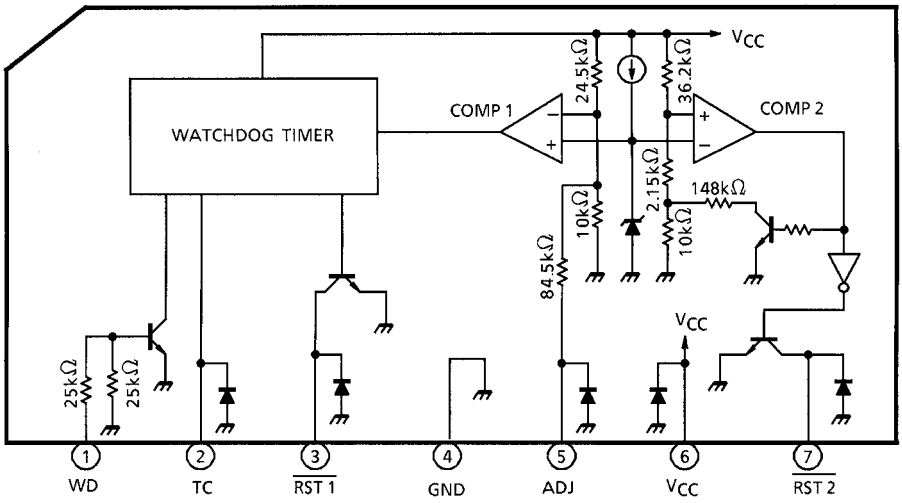
Weight
SIP7- P-2.54A : 0.7g (typ.)
SOP8- P-225-1.27 : 0.08g (typ.)

FEATURES

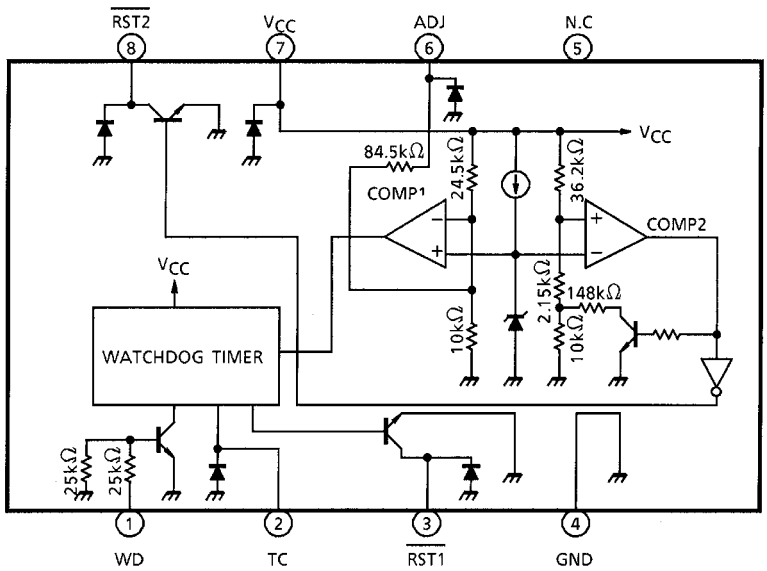
- Watchdog timer
- Power-on reset timer
- Dual-reset output
- SIP7 PIN (TA8030S)
  SOP8 PIN (TA8030F)

BLOCK DIAGRAM AND PIN LAYOUT

TA8030S



TA8030F



Note: The TA8030S and TA8030F are the same chip; only the packages are different.

PIN DESCRIPTION

PIN No.		SYMBOL	DESCRIPTION
TA80305	TA8030F		
1	1	WD	Clock input pin for watchdog timer. If this IC is only used as a power-on reset timer, this pin is connected to $\overline{RST1}$.
2	2	TC	Time setting pin for the reset and watchdog timers. R_1 leads to V_{CC}, and C_1 leads to GND.
3	3	$\overline{RST1}$	Supplies an NPN transistor open-collector output. ● Generates a reset signal determined by the CR combination connected to the TC pin. ● Supplies reset pulses intermittently if no clock is given to the WD pin.
4	4	GND	Grounded
5	6	ADJ	V_{CC} detect voltage (1) adjusting pin. The detection voltage is 4.6V when this pin is grounded ; it is 3.5V when this pin is directly connected to V_{CC}.
6	7	V_{CC}	Power supply pin for internal circuit. The output voltage can also be detected at this pin.
7	8	$\overline{RST2}$	Supplies an NPN transistor open-collector output. It is the output pin for V_{CC} detect voltage (2) . The detect voltage has a hysteresis of 0.17V.
—	5	NC	Not connected pin.(Electrically,this pin is completely open.)

FUNCTIONAL DESCRIPTION

About reset timer operation (See the timing chart)
The following explains the TA8030S/F's voltage monitoring and reset timer operations and how to use these functions.

(1) Voltage monitoring function (1)

The power input V_{CC} pin of this IC also serves as a voltage detection pin. When the V_{CC} voltage exceeds 4.25V after the IC is powered on, the power-on reset timer starts operating from that point in time. When the IC is powered off and V_{CC} drops below 4.25V, TC starts discharging and a reset signal is output when the voltage drops below 40% of V_{CC}. Also, if V_{CC} goes down for some reason during normal operation, a reset signal is output in the same way as described above, and when V_{CC} is up again and exceeds 4.25V, the power-on reset timer starts operating from that point in time.
The reset signal is forwarded to the $\overline{RST1}$ pin.

(2) Voltage monitoring function (2)

The $\overline{RST2}$ pin outputs a high when the V_{CC} voltage rises above 4.65V and outputs a low when it falls below 4.48V. This function only monitors the voltage operating independently of Voltage monitoring function (1) and the reset timer function. Since when the voltage drops the $\overline{RST2}$ output is inverted before a system reset signal is output from $\overline{RST1}$, this function can be used to inhibit writing to memory.
Also, this voltage detection has 3 μ s of response delay, td2, to prevent a reset from being generated inadvertently by minute noise. (For td2, refer to AC Electrical Characteristics.)

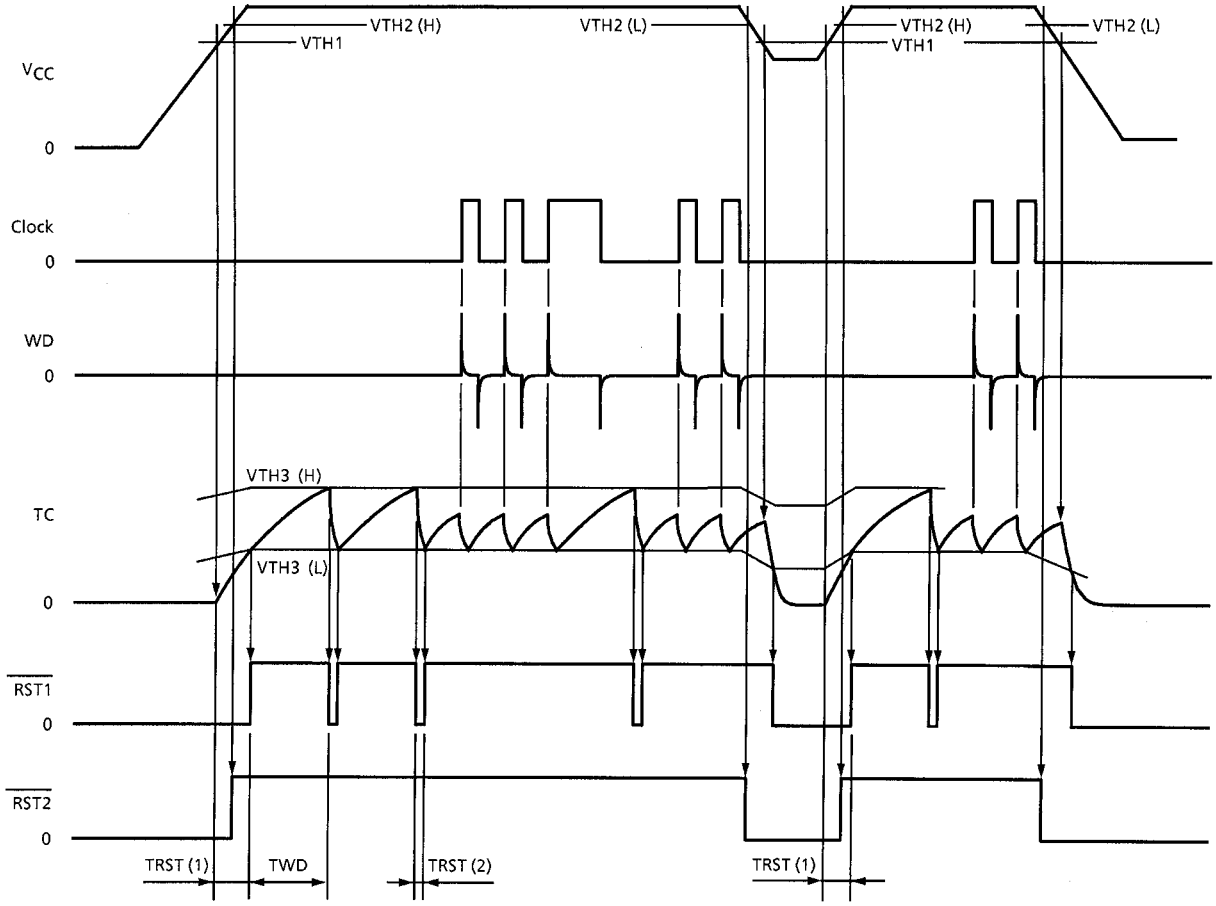
(3) Power-on reset timer function

The device is held in a reset state for a predetermined time until the 5V constant voltage stabilizes at power-on and until the oscillating clock of the CPU, etc. stabilizes before being freed from the reset state. This time can be set to any desired duration by using the appropriate resistor and capacitor values connected external to the TC pin.
When the V_{CC} voltage exceeds 4.25V, the system starts charging the capacitor and when this charging voltage exceeds 2V, the reset signal is inverted to deactivate the reset.

(4) Watchdog timer function

The WD pin between the CPU system and this IC is connected with an differential circuit. This is to ensure that when a failure occurs in the CPU system, a low signal is input to the WD pin no matter whether the clock output has stopped in the high or the low state. When the WD pin is fixed high, the watchdog timer stops operating.
If only the power-on reset timer is needed in your system, connect the WD pin to $\overline{RST1}$.

TIMING CHART



Note : See Electrical Characteristics for symbols in the timing chart.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	17	V
Input Voltage	$V_{IN\ (CK)}$	−7～7	V
Output Voltage	V_{OUT}	7	V
Output Current	I_{OUT}	10	mA
Power Dissipation	P_D	300/280	mW
Operating Temperature	T_{opr}	−40 to 85	℃
Storage Temperature	T_{stg}	−55 to 150	℃
Lead Temperature-time	T_{sol}	260 (10s)	℃

Note: P_D : TA8030S/TA8030F

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = −40 to 85°C)

(1) DC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	PIN	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Current	I_{IH}	WD	1	V_{IN} = 5V	0.1	0.17	0.35	mA
	I_{IL}		1	V_{IN} = −5V	−0.06	−0.1	−0.2	
Input Voltage	V_{IH}	WD	2	—	2.2	—	—	V
	V_{IL}		2	—	—	—	0.6	
Input Current	I_{IN}	TC	4	V_{IN} = 1.5V	−2	—	2	μA
Output Current	I_{OUT}	TC	4	V_{OUT} = 4.2V	2.4	4	7.7	mA
Watchdog Timer Threshold Voltage	$V_{TH3\ (H)}$	TC	3	—	3.5	4	4.5	V
	$V_{TH3\ (L)}$		3	—	1.75	2	2.25	
Output Voltage	V_{OL}	$\overline{RST1}$	5	I_{OUT} = 2mA	—	—	0.5	V
Output Leakage Current	I_{LEAK}	$\overline{RST2}$	6	V_{OUT} = 7V	—	—	5	μA
V_{CC} Detect Voltage (1)	V_{TH1}	V_{CC}	—	—	4.0	4.25	4.5	V
	$V_{TH1\ (H)}$		3	AJD = GND	4.3	4.6	4.9	
	$V_{TH1\ (L)}$		3	ADJ = V_{CC}	3.25	3.5	3.75	
V_{CC} Detect Voltage (2)	$V_{TH2\ (H)}$	V_{CC}	3	—	4.4	4.65	4.9	V
	Δ_{VTH2}		3	—	—	0.17	0.3	
Current Consumption	I_{CC}	V_{CC}	7	—	—	2.5	4.5	mA

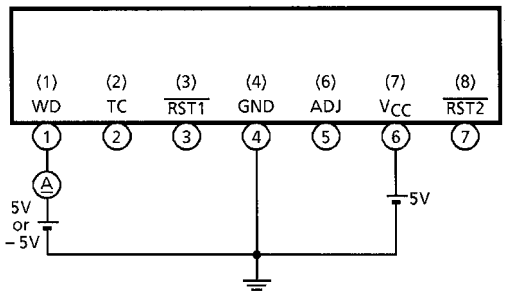
(2) AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	PIN	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Watchdog Timer	T_{WD}	$\overline{RST1}$	3		0.9 × C1R1	1.1 × C1R1	1.3 × C1R1	ms
Reset Timer (1)	$T_{RST\ (1)}$	$\overline{RST1}$	3		0.4 × C1R1	0.5 × C1R1	0.6 × C1R1	ms
Reset Timer (2)	$T_{RST\ (2)}$	$\overline{RST1}$	3		0.35 × C1	0.75 × C1	1.5 × C1	ms
Input Pulse Width	T_W	WD	3		3	—	—	μs
Transfer Delay Time	t_{d1}	$\overline{RST1}$	3	t_{dHL} (C1 = 0μF)	—	3	10	μs
	t_{d2}	$\overline{RST2}$	3	t_{dHL}, t_{dLH}	—	3	10	

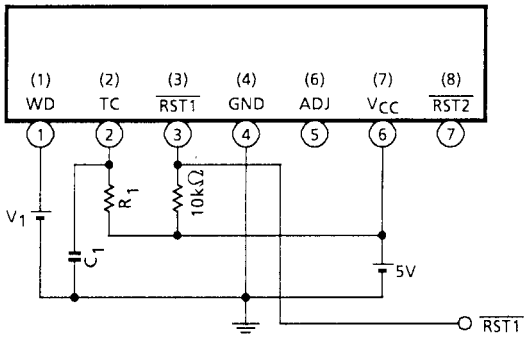
Note: The unit for the C1 is μF、the unit for R1 is kΩ.

TEST CIRCUIT (Number in ○ show pin number of the TA8030S, those in ( ) show pin number of the TA8030F.)

1. I_{IH}、I_{IL} (WD)

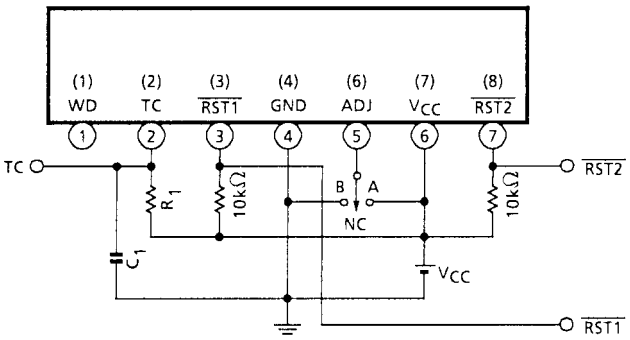


2. V_{IH}、V_{IL} (WD)



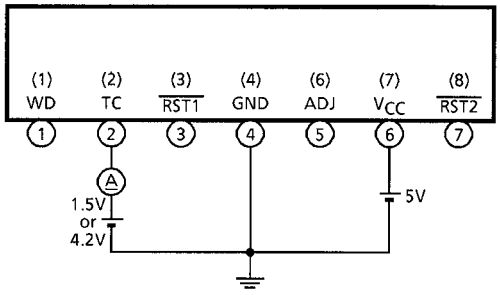
At $V_1 = 2.2V$, $\overline{RST1}$ must be 5V.
At $V_1 = 0.6V$, $\overline{RST1}$ must generate a Pulse signal.

3. $V_{TH3\,(H)}$、$_{(L)}$ (TC)、V_{TH1}、$V_{TH1\,(H)}$、$_{(L)}$、$V_{TH2\,(H)}$、ΔV_{TH2}、AC CHARACTERISTICS

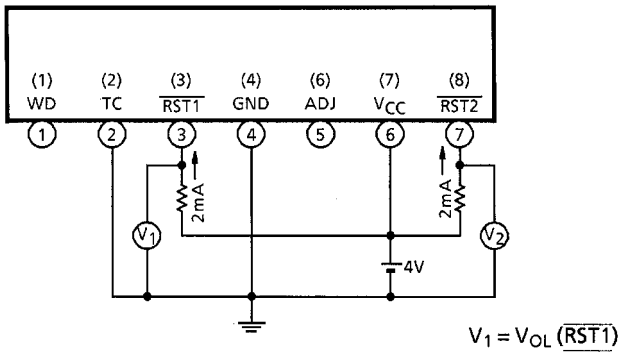


∴ See Timing Chart
$\Delta V_{TH2} = V_{TH2\,(H)} - V_{TH2\,(L)}$

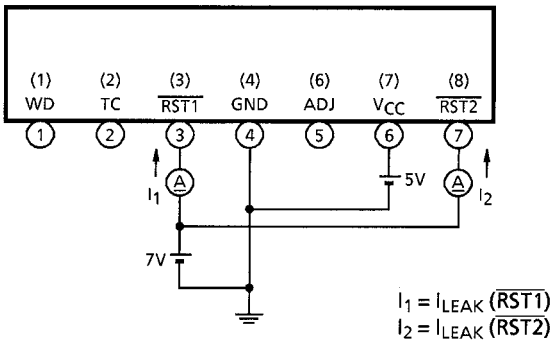
4. I_{IN}、I_{OUT} (TC)



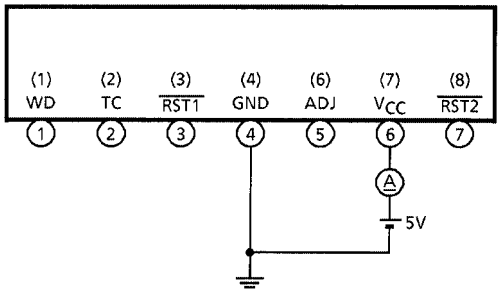
5. V_{OL} ($\overline{RST1}$) ($\overline{RST2}$)



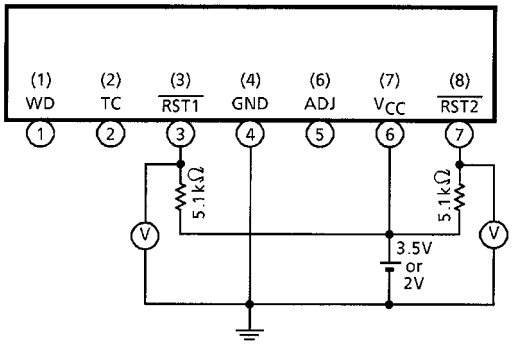
6. I_{LEAK} ($\overline{RST1}$) ($\overline{RST2}$)



7 I_{CC}

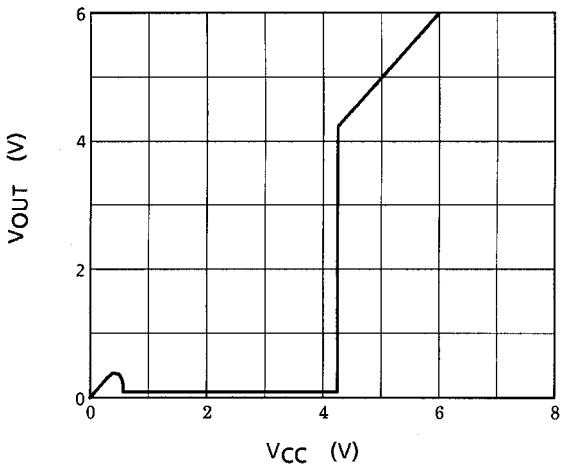


8. $V_{OL\ (1)、(2)}$ ($\overline{RST1}$) ($\overline{RST2}$)

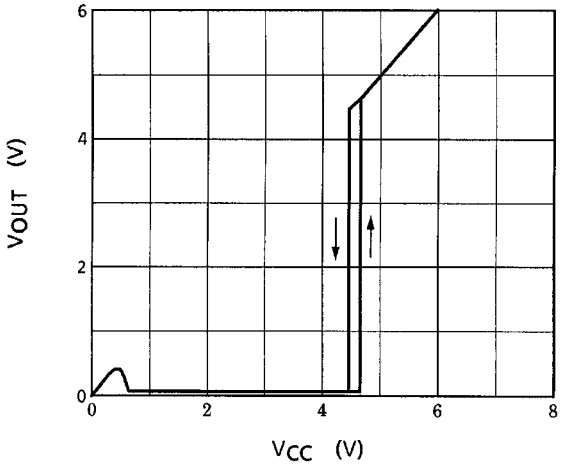


RESET OUTPUT STANDARD CHARACTERISTICS

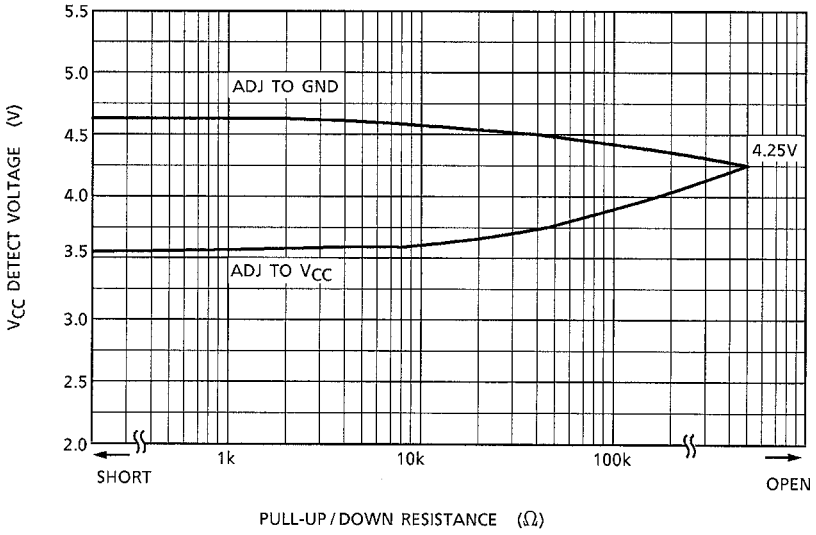
1. $\overline{\text{RST1}}$



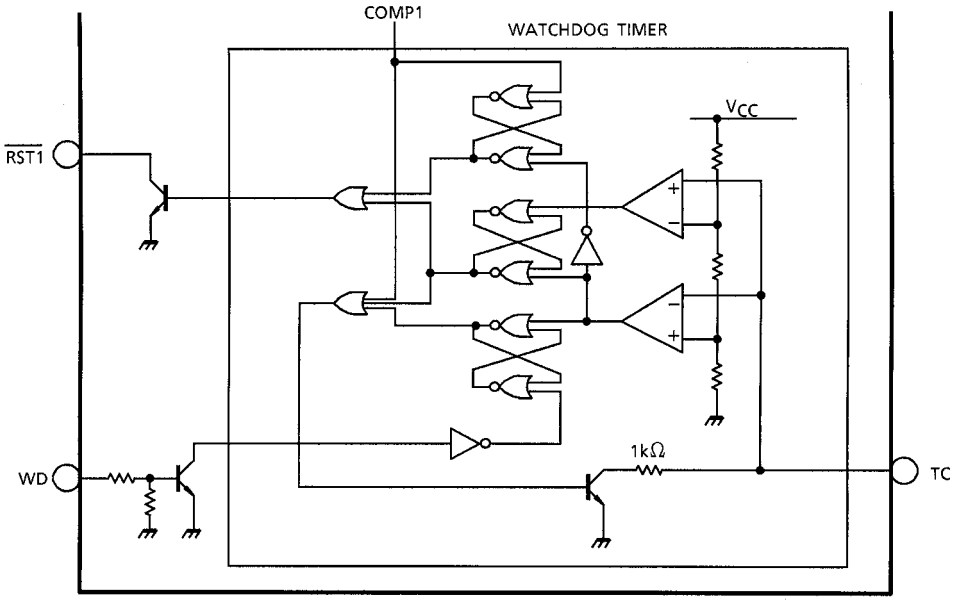
2. $\overline{\text{RST2}}$



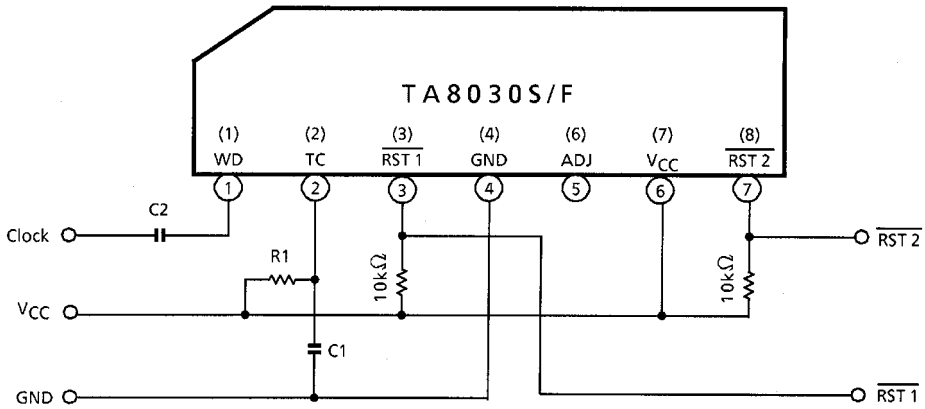
ADJ PIN PULL-UP / DOWN RESISTANCE VS VCC DETECT VOLTAGE



EQUIVALENT CIRCUIT DIAGRAM (WATCHDOG TIMER)



EXAMPLE OF APPLICATION CIRCUIT

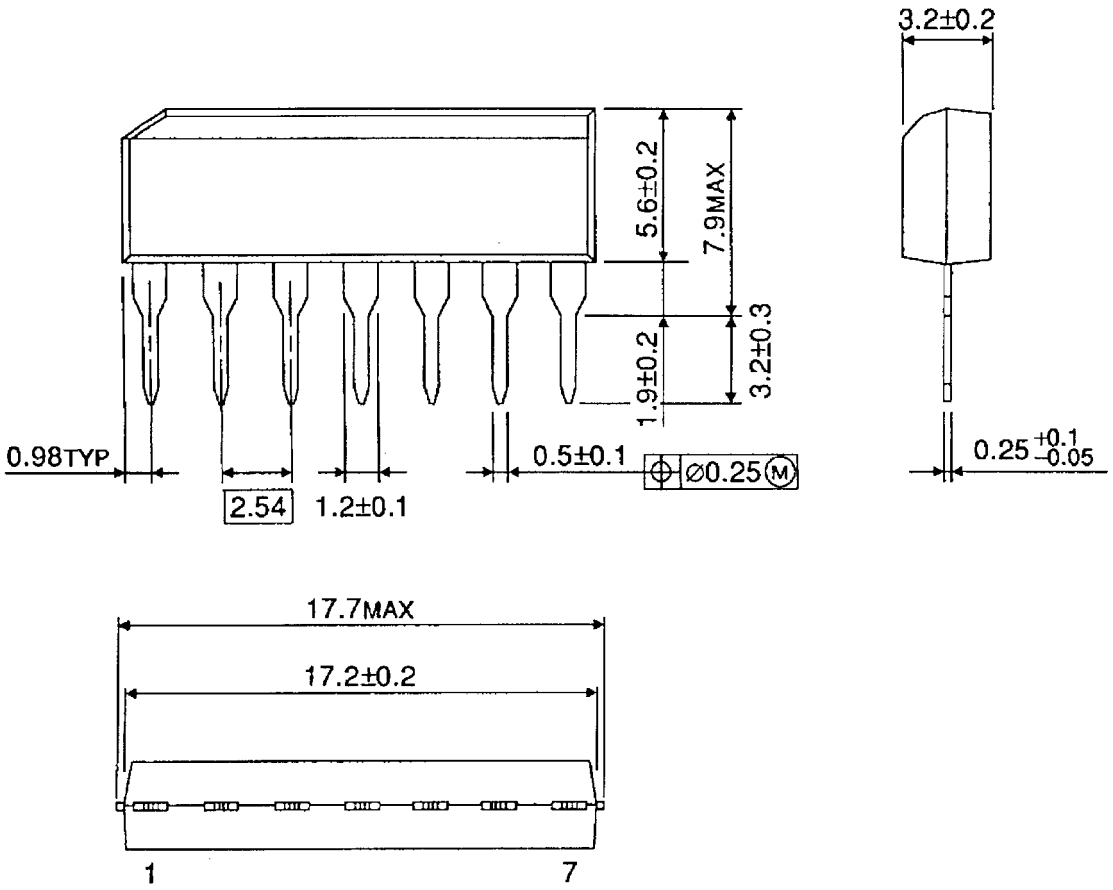


RECOMMENDED CONDITIONS

PART NAME	MIN	TYP.	MAX	UNIT
C_1	0.01		100	μF
R_1	10		100	kΩ
C_2		2200		pF

Package Dimensions

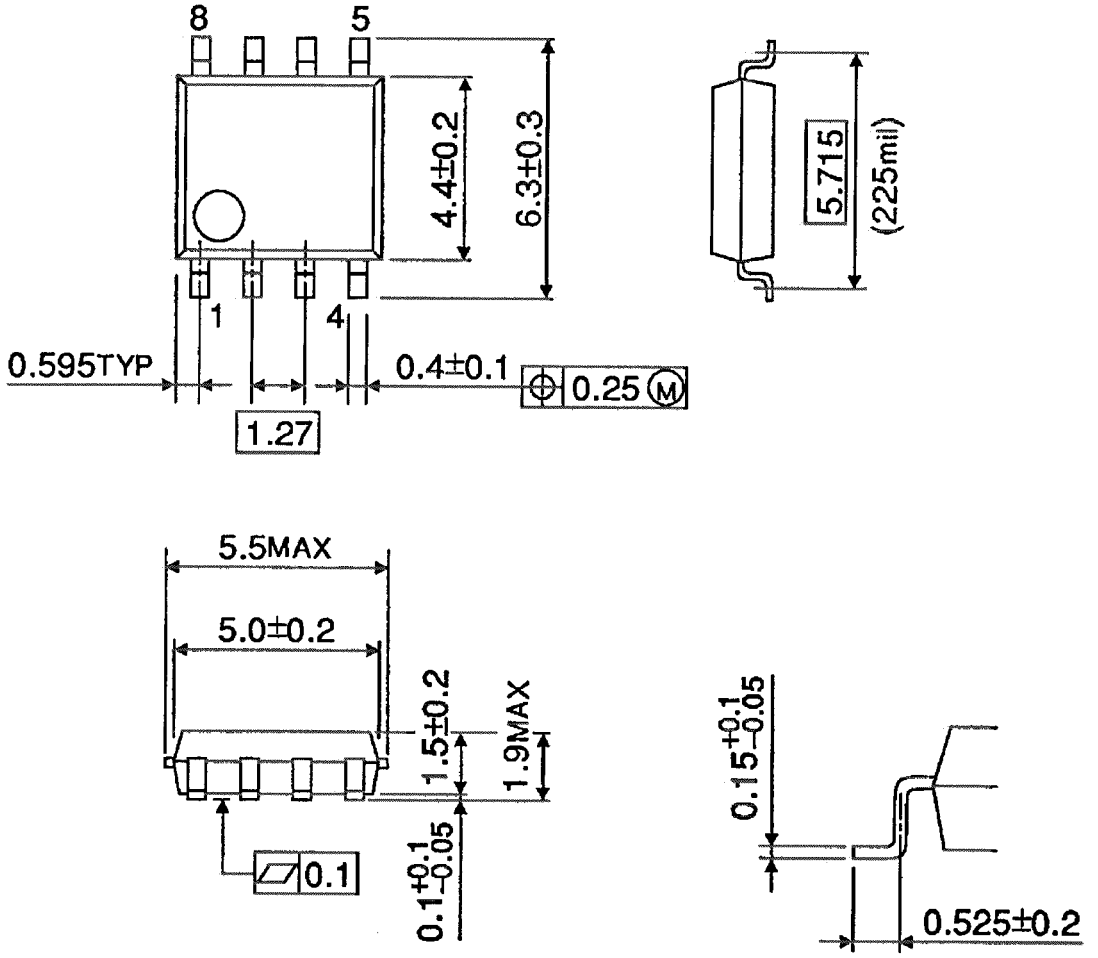
SIP7-P-2.54A Unit : mm



Weight: 0.7g (Typ.)

Package Dimensions

SOP8-P-225-1.27 Unit : mm



Weight: 0.08g (Typ.)

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